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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,162	07/28/2003	Sander L. Gierkink	S. GIERKINK 2-2	4343

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EXAMINER	
HANNON, CHRISTIAN A	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,162	GIERKINK ET AL.	
	Examiner	Art Unit	
	Christian A. Hannon	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is response to applicant's response filed on 10/10/2006. Claims 1-21 are now pending in the present application. **This action is made final.**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 8 & 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Jen et al (US 6,737,920), herein Jen.

Regarding claims 1 & 8, Jen teaches a phase-error suppressor for use with a plurality of transistors having a common source coupled to a current generator and configured to receive signals at a frequency, comprising an inductor, coupled between said common source and said current generator, configured to resonate proportionally to said frequency with a first capacitance associated with said plurality of transistors (Column 4, Lines 53-65; Figure 5C). Furthermore since claim 8 is merely a method recitation of claim 1, it is rejected on the same grounds.

In regard to claims 5 & 12, Jen teaches the phase-error suppressor as recited in Claim 1, further comprising a capacitor coupled to said inductor and coupled in parallel to a said current generator, said capacitor being configured to shunt said inductor to

ground at a selected radio frequency (RF) (Figure 5C, Items C_S, L_S). Furthermore since claim 12 is merely a method recitation of claim 1, it is rejected on the same grounds.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 6, 7, 9-11 &13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jen in view of Sano et al (US 5,884,154), herein Sano.

In regards to claims 2 & 9, Jen teaches the phase-error suppressor of claims 1 & 8, however Jen fails to teach wherein said plurality of transistors and said current generator form a portion of a system selected from a group consisting of a quadrature oscillator buffer, a quadrature oscillator and a quadrature mixer. Sano teaches a plurality of transistors and said current generator form a portion of a system selected from a group consisting of a quadrature oscillator buffer (Figure 1, Items 51, 53, VDD, Q1-4, 41, 43, 45, 47, 15, 19 & 25; Sano), a quadrature oscillator (Column 3, Lines 35-39; Sano) and a quadrature mixer (Column 3, Lines 25-27; Sano). Therefore it would have been obvious to combine a RF communication system out of Jen's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 9 is merely a method recitation of claim 2, it is rejected on the same grounds.

With regards to claims 3 & 10, Jen teaches the phase-error suppressor of claims 1 & 8, however Jen fails to teach wherein said inductor and said first capacitance resonate at twice said frequency. Sano teaches wherein said inductor and said first capacitance resonate at twice said frequency (Column 4, Lines 3-5, 10-12 and 23-44; Sano). Therefore it would have been obvious to combine a RF communication system out of Jen's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 10 is merely a method recitation of claim 3, it is rejected on the same grounds.

Regarding claims 4 & 11, Jen teaches the phase error suppressor of claims 1 & 8, however Jen fails to teach wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors. Sano teaches wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors (Column 3, Lines 39-45; Sano). Therefore it would have been obvious to combine a RF communication system out of Jen's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 11 is merely a method recitation of claim 4, it is rejected on the same grounds.

In regards to claims 6 & 13, Jen teaches the phase error suppressor of claims 1& 8, however Jen fails to teach wherein said frequency is at least three GHz. Sano teaches wherein said frequency is at least three GHz (Column 5, Lines 43-46; Sano). While Sano mentions in particular an example of an operating frequency of 880MHZ in one example (Column 5, Lines 9-19), he does not limit the operating frequency to this

particular specific frequency and goes on to teach the use of the circuit in a wireless telephone, obvious to one of ordinary skill in the art, which could operate at at least three GHz. Therefore it would have been obvious to combine a RF communication system out of Jen's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 13 is merely a method recitation of claim 6, it is rejected on the same grounds.

With regards to claims 7 & 14, Jen teaches the phase error suppressor of claims 1 & 8, however Jen fails to teach where said signals are four periodic local oscillator signals having a 90-degree phase difference. Sano teaches where said signals are four periodic local oscillator signals having a 90 degree phase difference (Column 2, Lines 33-35; Sano). Therefore it would have been obvious to combine a RF communication system out of Jen's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 14 is merely a method recitation of claim 7, it is rejected on the same grounds.

Regarding claims 15-21, therein recited are the limitations previously disclosed in apparatus and method claims 1-7 & 8-14, respectively, with the addition that the circuitry details are now made to comprise within an image-rejecting down-converter for use with a RF receiver. Jen or Jen in combination with Sano teaches all the limitations as previously rejected above in addition to the circuit being used within an image-rejecting down-converter for use with an RF receiver (Column 5, Lines 43-46; Sano) obvious to one of ordinary skill in the art Jen would be applied to a receiver structure and therefore one would be motivated to implement the teachings of Sano with Jen to

form an image rejected down converter in order to add the benefit of lower noise in the receiver.

Response to Arguments

5. Applicant's arguments filed 10/10/2006 have been fully considered but they are not persuasive.

The Applicant contends that Jen does not teach an inductor coupled between the common source and the current generator and causing the inductor to resonate proportionally to the frequency of the received signals with a first capacitance associated with the plurality of transistors to suppress a phase-error with the received signals (Page 3, Lines 19-20; Applicant Remarks/Arguments). The Examiner makes it of record that an inductor is operationally defined as something that introduces inductance; all inductors behave in the exact same manner. For that matter all transistors inherently have an associated capacitance. Extending this concept further all exact replicated circuit layouts behave in the same manner. Applying this concept to the Applicant's claim language with that of the prior art of Jen one will see that Jen discloses the exact circuit layout of the Applicant's claim language. Therefore Jen reads on the prior art, while the applicant wishes to argue that Jen doesn't explicitly say that the inductor resonates proportionally to a frequency existing in a capacitance associated with a transistor bank, Jen does not need to as this is inherently taking place based on the circuit design. Lastly the Examiner wishes to state that the preamble of the claim, which the Applicant has relied on in making their arguments (Page 4, Line 20

Page 5, Line 1; Applicant Remarks/Arguments), has not been given patentable weight because it merely recites the purpose of the structures intended use (See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie,* 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951)). For the reasons stated above claims 1 & 8 remain rejected, and subsequently all dependent claims remain rejected for the reasons cited within this action.

In regards to claims 5, 12 & 19, the Examiner maintains that since when the capacitor Cs of Jen pulls the circuit to ground it effectively creates a ground as the series of Ls and I bias are effectively put into a high impendence state which then would be pulled to the actively driven output, which in this instance would be ground or zero volts, therefore Jen reads on the currently recited claim language.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian A. Hannon whose telephone number is (571) 272-7385. The examiner can normally be reached on Mon. - Fri. 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian A. Hannon
December 18, 2006

12-19-06

LANA LE
PRIMARY EXAMINER